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EXAMINER	
CRAIG, DWIN M	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/459,995	CHALFIN ET AL	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-8,11,12,14 and 15* is/are rejected.

7)☒ Claim(s) *3, 4, 5, 9, 10 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-15 have been presented for reconsideration.

Response to Arguments

2. Applicant's arguments filed on 21 April 2003 have been fully considered. Examiners response is as follows:

2.1 Regarding Applicant's response concerning Examiner's claim interpretation:

Applicant has argued that:

> Applicants note the Examiner's remarks with respect to the terms "clock credit," "test bench," and "clock arbitrator" (Office Action, p. 2). Applicants submit that each of these terms has a clear plain meaning and is properly interpreted as being broad enough to include, but not be limited to, the examples provided throughout the specification and the example interpretation provided by the Examiner. While the Applicants do not acquiesce in the Examiner's interpretation, even if the Examiner's interpretation is accepted for the sake of argument, the Applicants contend that the invention is nonetheless patentable.

The Examiner asserts that the original claim language interpretations are correct in that they reflect the functionality of Applicant's claimed invention. The Examiner upholds the earlier claim interpretation as being valid.

2.2 Regarding Applicant's response to the 35 U.S.C. 103 rejections of Claims 1-5 and 11-13:

Applicant has argued that:

> Claims 1-5 and 11-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent 5,732,247 ("Dearth '247") in view of U.S. patent 5,790,829 ("Flynn"), and in further view of U.S. patent 5,363,319 ("Okuda") and in further view of the Microsoft Press Computer Dictionary, 3d Edition ("Microsoft") (Office Action, p. 3, sect. 4). Applicants respectfully traverse.
>
> These four references are not all applied by the Examiner to each of these rejected claims. Rather, these references are combined in different ways to particular claims.
>
> With respect to claim 1, the Examiner argues that this claim is rendered obvious by a combination of Dearth '247 and Flynn. The Examiner

argues that while Dearth '247 does not disclose issuing a clock credit or token to control simulation modules, Flynn discloses the use of a token to control module execution (Office action, pp3, 4).

As stated on page 6 of the specification for the present invention, a clock credit is a token issued to a simulation module and having a numerical value, permitting a device under test (DUT) to execute for some number of clock cycles associated with the value of the clock credit. Execution stops after the clock cycles have been used. Neither Flynn nor Dearth '247 discloses such a clock credit. While Flynn discloses "tag event structures" that mark the conclusion of processing of a family of "event structures," these tag event structures do not represent clock credits. Rather, tag event structures, according to Flynn, mark the completion of processing of previously-sent event structures (Flynn, column 9, lines 23-31). The tag event structures are used to mark checkpoints for synchronization purposes (Flynn, column 3, line 62- column 4, line 2). There is no disclosure in Flynn (or Dearth '247) of a tag or token that has a value associated with a number of clock cycles for which a simulation module is to execute. The issuance of a clock credit, as the term is used in the present application, is therefore **absent from Dearth '247 and Flynn**. The combination of these two references therefore fails to render claim 1 obvious. Moreover, claims 2-5 depend from claim 1 and necessarily incorporate all the limitations described in claim 1. Claims 2-5 are therefore patentable for at least the same reason as claim 1 and further in view of their own at least this reason, none of claims 1-5 are obvious in view of the cited art, taken alone or in combination.

Upon further review, the Examiner asserts that the *Flynn* appears to be deficient in teaching the issuance of a clock credit however the *Flynn* reference does disclose the presence of a data structure being passed to the simulation process. In view of the deficiency of the *Flynn* reference teaching the Applicant's disclosed limitations the Examiner withdraws the earlier 35 U.S.C. 103 rejection of Claims 1-5.

We note that the Examiner has rejected claim 3 as obvious in view of Dearth '247 and Flynn, and further in view of Okuda (Office Action, pp. 4, 5). Okuda, however, fails to overcome the shortcomings of Dearth '247 and Flynn with respect to the clock credit issuance limitation of claim 1. For at least this reason, claim 3 is not obvious in view of the cited art, taken alone or in combination.

The Examiner has also rejected claims 4 and 5 as obvious in view of Dearth '247 and Flynn, and further in view of Microsoft (Office Action, p.5). Microsoft, however, fails to overcome the shortcomings of Dearth '247 and Flynn with respect to the clock credit issuance limitation of claim 1. For at least this reason, neither of claims 4 and 5 is obvious in view of the cited art, taken alone or in combination.

The Examiner asserts that the rejections of Claims 3, 4 and 5 are withdrawn ONLY because of the shortcomings of the *Flynn* reference. *(See paragraph above.)*

2.3 Regarding Applicant's response to Examiner's rejection of independent Claim 11 and dependent Claim 13:

Applicant has argued that:

> Claim 11 is a computer program product claim that recites computer readable program code logic for causing a computer to execute the steps of method claim 1. The Examiner argues that claim 11 is rendered obvious by a combination of the Dearth '247 and Flynn references. As discussed above, however, the issuance of a clock credit to a simulation module is not disclosed by either Dearth '247 or Flynn, taken alone or in combination. Likewise, computer readable program code logic for causing a computer to issue a clock credit is not disclosed. For at least this reason, therefore, claim 11 is not rendered obvious by a combination of Dearth '247 and Flynn. Moreover, claims 12 and 13 depend from independent claim 11 and necessarily incorporate the limitations specified in claim 11. The limitation of computer readable program code logic for causing a computer to issue a clock credit is therefore present in claims 12 and 13, but 995 not disclosed by either Dearth '247 or Flynn. For at least this reason, therefore, claims 12 and 13 are not obvious over the art cited by the Examiner.

The Examiner asserts that due to the fact that the *Flynn* reference does not appear to disclose the limitation of issuing a clock credit, the Examiner withdraws the earlier 35 U.S.C. 103 rejection of Claim 11.

> The Examiner has rejected claim 13 as obvious in view of Dearth '247 and Flynn, and further in view of Okuda (Office Action, pp. 4, 5). Okuda, however, fails to overcome the shortcomings of Dearth '247 and Flynn with respect to the clock credit issuance limitation of claim 11. For at least this reason, claim 13 is not obvious in view of the cited art, taken alone or in combination.

The Examiner asserts that for the same reasons listed above the earlier 35 U.S.C. 103 rejections of independent Claim 11 and therefore dependent Claim 13 is withdrawn due to the apparent deficiency of the *Flynn* reference in not teaching a clock credit.

2.4 Regarding Applicant's response to the 35 U.S.C. 103 rejection of Claims 6, 7, 14 and 15:

Applicant has argued that:

Claims 6, 7, 14, and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patents 5,905,883 ("Kasuya") and 5,081,601 ("Eirikasson") and further in view of Microsoft. With respect to claim 6, the Examiner argues that this claim is rendered obvious by a combination of Kasuya and Eirikasson. In particular, the Examiner argues that Kasuya discloses the steps of reading the specification information, identifying a device under test, and determining the interface to the DUT (Office Action, pp. 5, 6). Kasuya, however, does not disclose these steps. Kasuya discloses a test bench that performs stimulus generation and output comparisons (Kasuya, col. 2, lines 1, 2), but never discusses steps for creating a test bench, apart from creation and compilation of a test bench source file (Kasuya, col. 4, line 66 through col. 5, line 2). Eirikasson likewise fails to disclose these steps. Eirikasson discloses interconnection and coordination of simulators (Eirikasson, col. 4, lines 13-29), but never addresses steps for creating a test bench. Kasuya and Eirikasson, either alone or in combination, therefore fails to render claim 6 obvious. Claim 7 depends from independent claim 6, and necessarily includes all the limitations of claim 6. Because a combination of Kasuya and Einkasson fails to disclose all the limitations of claim 6, it likewise fails to disclose all the limitations of claim 7. Claim 7 is therefore not obvious in view of the cited art.

The Examiner asserts that the creation of a *"test bench"* is known in the art as compiling a stimulus file. The stimulus file is created in the Hardware Description Language that the designer is currently using to design a circuit; once the file has been properly annotated the file is compiled into the design for testing during the simulation phase of the design process. The Examiner has found Applicant's arguments to be unpersuasive and upholds the earlier 35 U.S.C. 103 rejections of Claims 6, 7, 14 and 15.

Claim 14 is a computer program product claim that recites computer readable program code logic for causing a computer to perform the steps of claim 6. While the Examiner argues that a combination of Kasuya and Eirikasson renders claim 14 obvious (Office Action, p. 6), this combination fails to disclose the limitations pertaining to identification of a DUT, determination of an interface to a DUT, and generation of a test bench component for the DUT. Kasuya discloses a test bench that performs stimulus generation and output comparisons (Kasuya, col. 2, lines 1, 2), but never discusses program code logic for creating a test bench, apart from creation and compilation of a test bench source file (Kasuya, col. 4, line 66 through

col. 5, line 2). Eirikasson likewise fails to disclose program code logic for these steps. Eirikasson discloses interconnection and coordination of simulators (Eirikasson, col. 4, lines 13-29), but never addresses program code logic for creating a test bench. Kasuya and Eirikasson, either alone or in combination, therefore fails to render claim 14 obvious.

With respect to claim 14, the Examiner also states that Microsoft discloses computer readable code that is executed from a computer readable medium (Office Action, pp. 6, 7). This reference, however, fails to overcome the shortcomings of Kasuya and Eirikasson with respect to program code logic that identifies a DUT, determines an interface to a DUT, and generates a test bench component. Kasuya, Eirikasson, and Microsoft, either alone or in combination, therefore fail to render claim 14 obvious.

Because claim 15 depends from claim 14 and incorporates all the limitations of claim 14, claim 15 is likewise is not rendered obvious by this combination of references.

The Examiner asserts that detecting and establishing communication between a DUT and a software simulation is disclosed in the *Kasuya* reference *(see Figure 1, item 112 is the Device Under Test and the mechanism for detection and the determination for the interface is made by the programmer who creates the API Item 110, therefore detection and determination are inherent)*. The Examiner asserts that a (Device Under Test) can be a computer-based model as disclosed in **(Col. 1 Lines 62-65 U.S. Patent 5,905,883 *Kasuya*).** The Examiner asserts that based on the Applicant's claim language, wherein there is no specific definition of the *type* of Device Under Test, the *Kasuya* reference discloses the claimed limitations. The Examiner has found Applicant's arguments to be unpersuasive and upholds the earlier rejection of Claims 14 and 15.

2.5 Regarding Applicant's response to the 35 U.S.C. 103 rejections of Claims 8-10:

Applicant has argued that:

The Examiner has rejected claims 8-10 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,115,823 ("Velasco") in view of U.S. Patent 5,848,236 ("Dearth '236") and further in view of the article "VHDL for Programmable Logic" ("Skahill") and further in view of U.S. Patent 5,603,015 ("Kurosawa") (Office Action, p. 7).

In particular, the Examiner rejects claim 8 as being unpatentable over a combination of Velasco, Dearth '236, and Skahill. The Examiner argues that Velasco discloses the use of a clock arbitrator (Office Action, pp. 7, 8).

Velasco, however, fails to disclose a clock arbitrator wherein a programming language interface (PLI) receives a clock credit from the clock arbitrator. Moreover, while the Examiner argues that Skahill teaches a PLI, Skahill fails to teach a PLI that receives a clock credit from a clock **arbitrator**. Likewise, Dearth '236 fails to disclose these limitations. For at least these reasons, therefore, the combination of Dearth '236, Skahill, and Velasco fails to render claim 8 obvious. Because claims 9 and 10 depend from independent claim 8, claims 9 and 10 necessarily include all the limitations of claim 8. Because the cited art fails to disclose a clock arbitrator and a PLI that receives a clock credit from the clock arbitrator, the above combination of references fails to render claims 9 and 10 obvious.

With regard to claim 9, **the Examiner** also argues that Kurosawa discloses a shared memory interface (Office Action, p. 8). Kurosawa, however, fails to compensate for the shortcomings of Dearth '236, Skahill, and Velasco with respect to the limitations of a clock arbitrator and a PLI, wherein the PLI receives a clock credit from the clock arbitrator. Hence claim 9 is not obvious in view of Dearth '236, Skahill, Velasco, Kurosawa, or any combination thereof.

The Examiner asserts that the *Velasco et al.* reference is deficient in that it does not disclose a clock credit. The Examiner withdraws the earlier 35 U.S.C. 103 rejections of Claims 8-10 for the reason cited above.

Claim Interpretation

3. The claims have been given the broadest interpretation by the examiner. For the purposes of examination the examiner has determined that the term *"Clock Credit"* refers to the use of a data structure that is passed from a simulation control module and different executing simulation modules for the purpose of determining how many clock cycles that particular simulation module will execute and is therefore a *Token* or *Tag* that is used to determine which simulation module is currently executing and for how many clock cycles that module will execute (Specification page 3). For purposes of examination the examiner has determined that the term *"test bench"* refers to the set of test signals that are used as inputs to stimulate a circuit under simulation testing (Specification, pages 3 & 4). For purposes of examination the examiner has determined that the term *Clock arbitrator* is any type of Master Clock or Central Control module

that controls the distribution of clock signals throughout a simulation module (Specification Page 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dearth et al. U.S. Patent 5,732,247** in view of **Klein et al. U.S. Patent 5,768,567.**

4.1 As regards **Claim 1** the *Dearth et al.* reference discloses, a method of synchronizing a plurality of simulation modules **(Figure 1 and Col. 2 Lines 21-62, Col. 13 Lines 15-35, Col. 19 Lines 13-14);** ***(a)*** initializing a simulation module **(Figure 4a-d, and Col. 5 Lines 17-27, Col. 6 Lines 54-57, Col. 15 Lines 25-37),** by sending a MSG packet **(Figure 2),** ***(b)*** execution corresponding to an extent determined by the reception of a packet from the Comm Interface Core **(Figure 1 Items 20,21 and 23), (Figure 3, Figure 4C Item 115 and Col. 4 Lines 32-49, Col. 5 Lines 8-40),** ***(c)*** halting execution when the testing for that simulation module has been completed **(Figure 3 Items 61, 62, 63, Figure 4A Item 108, Figure 4B Item 109 and Col. 2 Lines 20-63, Col. 5 Lines 40-49),** ***(d)*** when additional processing by at least one simulation module s necessary, issuing a further MSG packet to each simulation module, **(Figure 3 Item 64**

and Figure 4C and Figure 4D Item 121 and Col. 4 Lines 32-49, Col. 5 Lines 40-57, Col. 8 Lines 32-39, Col. 9 Lines 24-44).

The *Dearth et al.* reference does not expressly disclose issuing a *Clock Credit* or *Token* to control the different simulation modules, although the MSG packet disclosed in **Figure 2** of the *Dearth et al.* reference effectively performs some of the functions of a control Token, *i.e. the transfer of control information.*

The *Klein et al.* reference discloses issuing a Clock Credit to control different simulation modules **(Figures 7, 10 ITEM 238, Figure 14, Col. 5 Lines 8-22, Col. 10 Lines 58-67, Col. 11 lines 1-11).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Dearth et al.* reference with the *Klein et al.* reference because, *(motivation to combine)* the *Klein et al.* reference discloses an improved method to simulate hardware and software at the same time, having this capability will result in a superior design simulation and therefore reduce the likelihood of a design flaw being introduced into an ASIC design. *As an example*, when designing any type of micro-processor or instruction processing device, the ability to model the interaction of executing instructions as well the reading and writing of data and instructions to and from main memory and, in particular, modeling the effects on the processor design when an instruction that requires several clock cycles to execute and then monitoring the effects on the processor's data, address and control bus when the associated directional controller's gates are tri-stated, it is essential to confirming that the design is sound and verifying that the processor is functioning well before the design is sent to a chip foundry and large amounts of time and resources (*money*) are expended to fabricate the ASIC. It is noted

by the Examiner that the *Klein et al.* reference is issued in the **703/13** subclass which in entitled **"DATA PROCESSING: STRUCTURAL DESIGN, MODELING, SIMULATION AND EMULATION/SIMULATING ELECTRONIC DEVICE OR ELECTRICAL SYSTEM"**, the Examiner asserts that it would be reasonable to assume that any artisan, in this area of art would have been aware of this reference and that because of the competitive nature of this area of technology, would have been motivated to understand the existing technology so as to not waste precious time and resources re-inventing an already existing technology.

4.2 As regards **Claim 2** the *Dearth et al.* reference discloses synchronization points identified in data passing between the simulation modules **(Figure 2 Items 41-46 and Figure 4B Item 109 and all of Figures 4C-D and Col. 2 Lines 21-63, Col. 4 Lines 24-28, Col. 6 Lines 54-58).**

5. **Claims 11 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dearth et al. U.S. Patent 5,732,247** in view of **Klein et al. U.S. Patent 5,768,567** and in further view of **Microsoft Press Computer Dictionary, Third Edition, *Published 1997*** here after referred to as the *Microsoft* reference.

5.1 As regards the limitations of **Claim 11** that are shared by **Claim 1** see the rejection in paragraph **4.1** above.

As regards the limitation in **Claim 11** concerning the use of computer readable executable code, the *Microsoft* reference discloses computer readable code being executed from a computer readable medium **(Pages 81, 82, 145, 146, 182 183, 201).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Dearth et al.* reference with the *Microsoft* reference because storing and executing software programs from computer readable media eliminates the requirement to manually enter the software program instructions every time a computer user wishes to execute the method described in Applicants application.

5.2 As regards **Claim 12** the *Dearth et al.* reference discloses synchronization points identified in data passing between the simulation modules **(Figure 2 Items 41-46 and Figure 4B Item 109 and all of Figures 4C-D and Col. 2 Lines 21-63, Col. 4 Lines 24-28, Col. 6 Lines 54-58).**

6. **Claims 6, 7, 14 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kasuya U.S. Patent 5,905,883** in view of **Eirikasson U.S. Patent 5,081,601** and in further view of **Microsoft Press Computer Dictionary, Third Edition, *Published 1997*** here after referred to as the *Microsoft* reference.

6.1 As regards **Claims 6 and 14** the *Kasuya* reference discloses, creating a test bench component of a simulation module comprising the steps of reading specification information, identifying the DUT, determining the interface to the DUT, **(Figure 1 Item 130 and Figure 2 and Col. 1 Lines 1-67, Col. 2 Lines 1-67, Col. 3 Lines 1-67, Col. 4 Lines 59-67 and Col. 5 Lines 1-64).**

The *Kasuya* reference does not expressly disclose supporting testing of a plurality of time domains.

The *Eirikasson* reference discloses a plurality of time domains **(Figure(s) 1-6 and Col. 4 Lines 13-30).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Kasuya* reference with the *Eirikasson* reference because, *(motivation to combine) by synchronizing two independently clocked simulators peak performance is maintained* ***(Eirikasson reference Col. 3 Lines 58-67 and Col. 4 Lines 1-30).***

6.2 As regards **Claims 7 and 15** the *Kasuya* reference discloses determining the inputs and outputs of the DUT, ascertaining the attributes of said inputs and outputs and deriving the protocols of said inputs and outputs **(Figures 1-4 and Col. 1 Lines 53-65).**

6.3 As regards **Claim 14** the *Microsoft* reference discloses computer readable code being executed from a computer readable medium **(Pages 81, 82, 145, 146, 182 183, 201).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Kasuya* reference with the *Microsoft* reference because storing and executing software programs from computer readable media eliminates the requirement to manually enter the software program instructions every time a computer user wishes to execute the method described in Applicants application.

7. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Velasco et al. U.S. Patent 6,115,823** in view of **Dearth et al. U.S. Patent 5,848,236** and in further view of **"VHDL for Programmable Logic" by Kevin Skahill** *hereafter referred to as the Skahill reference* and in further view of **Klein et al. U.S. Patent 5,768,567.**

7.1 As regards **Claim 8**, the *Velasco et al.* reference discloses the use of a clock arbitrator to synchronize several computer sub-system modules **(Figure 1 Item 25 and Figure 2 Item 130, 53a, 53n and Figure 3 and Figure 11 all of Item 130 and all of Figure 12 and Figure 21 Items 248 and 249 and the rest of Figure 21 and Figure 26 and 27 and Figure 30 and all of Figure 47 and Col. 25 Lines 25-67, Col. 32 Lines 18-48, Col. 33 Lines 34-40, Col. 42 Lines 26-65).**

The *Velasco et al.* reference does not expressly disclose: synchronizing a plurality of simulation modules, a programming language interface, a test bench or a device under test.

The *Dearth et al.* reference discloses synchronizing multiple simulation modules **(Figures 1-20 and Col. 2 Lines 20-60).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Velasco et al.* reference with the *Dearth et al.* reference because, ***...the invention provides structure and method for a modular bus architecture (MBA) and fast modular bus archetechure (FMBA) frames for System-on-a-Chip (SOC) designs including MBA/FMBA library modules that decrease design time. (Velasco et al. Col. 4 Lines 49-54).***

The *Skahill* reference discloses a programmable language interface, a test bench and a device under test **(Skahill, Pages 541-543 and Figure 10-1).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Velasco et al.* reference with the *Skahill* reference because, ***...the invention provides structure and method for a modular bus architecture (MBA) and fast modular bus archetechure (FMBA) frames for System-on-a-Chip (SOC) designs including MBA/FMBA library modules that decrease design time. (Velasco et al. Col. 4 Lines 49-54).***

The *Velasco et al.* reference does not expressly disclose a clock credit.

The *Klein et al.* reference discloses issuing a Clock Credit to control different simulation modules **(Figures 7, 10 ITEM 238, Figure 14, Col. 5 Lines 8-22, Col. 10 Lines 58-67, Col. 11 lines 1-11).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Velasco et al.* reference with the *Klein et al.* reference because, *(motivation to combine)* the *Klein et al.* reference discloses an improved method to simulate hardware and software at the same time, having this capability will result in a superior design simulation and therefore reduce the likelihood of a design flaw being introduced into an ASIC design. *As an example*, when designing any type of micro-processor or instruction processing device, the ability to model the interaction of executing instructions as well the reading and writing of data and instructions too and from main memory and, in particular, modeling the effects on the processor design when an instruction that requires several clock cycles to execute and then monitoring the effects on the processor's data, address and control bus when the associated directional controller's gates are tri-stated, it is essential to confirming that the design is sound and verifying that the processor is functioning well before the design is sent to a chip foundry and large amounts of time and resources (*money*) are expended to fabricate the ASIC. It is noted by the Examiner that the *Klein et al.* reference is issued in the **703/13** subclass which in entitled "**DATA PROCESSING: STRUCTURAL DESIGN, MODELING, SIMULATION AND EMULATION/SIMULATING ELECTRONIC DEVICE OR ELECTRICAL SYSTEM**", the Examiner asserts that it would be reasonable to assume that any artisan, in this area of art would have been aware of this reference and that because of the competitive nature of

this area of technology, would have been motivated to understand the existing technology so as to not waste precious time and resources re-inventing an already existing technology.

Allowable Subject Matter

8. **Claims 3, 4, 5, 9, 10 and 13** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. An updated search has revealed new art. The Examiner withdraws the earlier rejections of **Claims 1-5, 11, 13, and 8-10**. The Examiner upheld the earlier rejections of **Claims 6, 7, 14 and 15.** The Examiner has applied new art rejections to **Claims 1, 2, 11, 12 and 8.** The Examiner is now objecting to **Claims 3, 4, 5, 9, 10 and 13** because they are dependent on rejected base claims.

9.1 This Office Action is **NON-FINAL** because of the new art rejections.

9.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
June 25, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER